REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 9-14 and 16-24 are currently pending. Claims 16, 21, and 22 have been amended by the present amendment. The changes to the claims are supported by the originally filed specification and do not add new matter.

In the outstanding Office Action, Claims 21 and 22 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,473,280 to Buxton et al. (hereinafter "the '280 patent"); Claims 16-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over "Applicants' admitted prior art" (hereinafter "the Background Art") in view of the '280 patent; and Claims 9-14, 23, and 24 were allowed.

Amended Claim 21 is directed to a semiconductor apparatus comprising a logic level decision circuit that is connected to a signal transmission line, the logic level decision circuit having a first reference signal having a logic "1" level and a second reference signal having a logic "0" level input as reference signals for deciding a logic level of an input signal input from the signal transmission line, and which decides the logic level of the input signal in accordance with which of the signal levels of the first and second reference signals the signal level of the input signal is close to. Further, Claim 21 clarifies that the first and second reference signals are inputted from outside of the semiconductor apparatus. The changes to Claim 21 are supported by the originally filed specification and do not add new matter.

Regarding the rejection of Claim 21 as anticipated by the '280 patent, the '280 patent is directed to a switching voltage regulator failure detection circuit that includes a clock generator, a driver circuit that drives an output transistor of a switching regulator on and off to conduct current to an output inductor; a decision circuit connected to sense a parameter that transitions above and below a predetermined threshold during each cycle of the clock

signal as the output transistors drift on and off; and a counter having a clock input connected to receive the clock signal and reset input connected to receive a decision circuit output. As shown in Figure 2a, the '280 patent discloses a switching regulator output stage 10 having an output terminal 14. Further, the '280 patent discloses that the output terminal is connected to a window comparator 44 that has signals V_{high} and V_{low} as inputs. Further, the '280 patent discloses that the "window comparator 44 toggles an output 44 when V_{out} falls outside the range defined by V_{high} and V_{low}."[1] Further, the '280 patent discloses that the signals V_{high} and V_{low} represent upper and lower boundaries for input signal 46.

However, Applicants respectfully submit that the '280 patent fails to disclose a logic level decision circuit that is connected to a signal transmission line. Rather, the '280 patent discloses that the circuit 44 is connected to the switching regulator output, which is different from the claimed signal transmission line.

Further, Applicants respectfully submit that the '280 patent fails to disclose that the logic level decision circuit decides the logic level of the input signal in accordance with which of the signal levels of the first and second reference signals the signal level of the input signal is close to, as recited in Claim 21. Rather, the '280 patent discloses that the circuit 44 determines whether the input signal 46 has fallen ***outside the range defined by V_{high} and V_{low}***. Thus, the output 48 disclosed by the '280 patent does not indicate which signal level the input signal is close to, as required by Claim 21. Rather, the output signal 48 merely indicates whether the input signal 46 is inside or outside the range defined by V_{low} and V_{high}. Accordingly, Applicants respectfully submit that amended Claim 21 patentably defines over the '280 patent.

Independent Claim 22 recites limitations analogous to the limitations recited in Claim 21. In particular, Claim 22 recites an input signal of a signal transmission line. Moreover,

[1] See column 5, lines 55-60.

Claim 22 clarifies that a third comparison circuit compares the output of a first comparison circuit and the output of a second comparison circuit and outputs one of the logic "1" level and the logic "0" level. Further, Claim 22 clarifies that the output of the third comparison circuit follows the external input signal.

Applicants respectfully submit that the '280 patent fails to disclose a third comparison circuit wherein the output of the third comparison circuit follows the external input signal that is input from the signal transmission line. As discussed above, the '280 patent does not disclose an input signal of a signal transmission line, but discloses a signal from a signal regulator stage. Further, as discussed above, the '280 patent discloses that the circuit 44 determines whether the input signal is inside or outside of the range defined by V_{low} and V_{high}. However, the circuit 44 does not disclose that the output of a third comparison circuit follows an external input signal, as required by Claim 22. Accordingly, for the reasons stated above, Applicants respectfully submit that amended Claim 22 patentably defines over the '280 patent.

Independent Claim 16 is directed to a signal transmission that transmits and receives binary logic signals between a plurality of semiconductor apparatuses, wherein the plurality of semiconductor apparatuses respectively have an input receiver that is connected to a signal transmission line, and the input receivers decides a logic level of an external input signal input from the signal transmission line, and a first reference signal corresponding to a logic "1" level of the input signal and a second reference signal corresponding to a logic "0" level are supplied as reference signals for logic level decision to the respective input receivers. Further, Claim 16 recites that the respective input receivers output one of the logic "1" level and the logic "0" level, and the output of the respective input receivers follows the external input signal.

Applicants respectfully traverse the rejection of Claim 16 as being unpatentable over the combine teachings of the Background Art and the '280 patent. As discussed above, the '280 patent fails to disclose that the output of an input receiver follows an external input signal that is input from a signal transmission line. The '280 patent does not disclose an input signal input from an signal transmission line and does not disclose that a signal follows the external input signal, as required by Claim 16. Rather, the '280 patent merely discloses that the output signal 48 from the circuit 44 merely indicates whether the input signal is inside or outside the range defined by V_{low} and V_{high}.

Applicants respectfully submit that the Background Art fails to remedy the deficiencies of the '280 patent in this regard. Moreover, Applicants note that the Office Action does not rely on the Background Art to disclose these limitations. Accordingly, Applicants respectfully submit that no matter how the teachings of the Background Art and the '280 patent are combined, the combination does not teach or suggest the limitations recited in amended Claim 16.

Thus, it is respectfully submitted that independent Claims 16, 21, and 22 (and all associated dependent claims) patentably define over any proper combination of the '280 patent and the Background Art.

Consequently, in view of the present amendment and in light of the above discussion, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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